

# Am2809

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

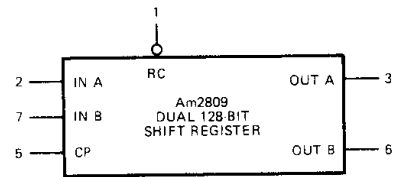
- Second source to Signetics 2521.
- TTL compatible on clock and data inputs.
- Operation guaranteed from DC-to-2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Low capacitance on clock and data inputs.

### FUNCTIONAL DESCRIPTION

The Am2809 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers have a common clock input which is low-threshold TTL compatible. The registers also have built-in recirculate feedback. When the recirculate control ( $\overline{RC}$ ) is LOW, the data on the data output of each register is fed back to the corresponding register input. When  $\overline{RC}$  is HIGH, each register accepts data from the data input. Each of the register outputs can drive one standard TTL load or three Am93L series low-power unit loads.

Data in the Am2809 is shifted on the LOW-to-HIGH edge of the input clock. Data on the data inputs must remain steady for a set-up time before and a hold time after this clock transition. Since storage in the register is static, the register may be halted indefinitely with the clock in the HIGH state.

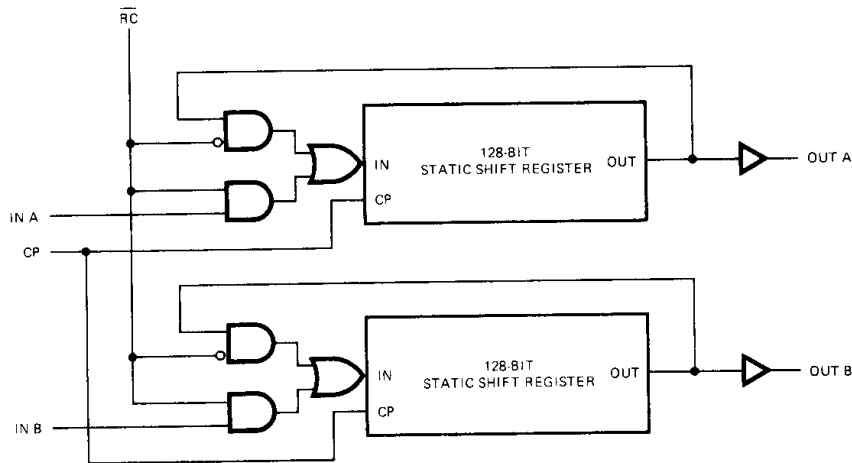
### LOGIC SYMBOL



$V_{CC}$  = Pin 8  
 $V_{GG}$  = Pin 4

MOS-403

### LOGIC BLOCK DIAGRAM



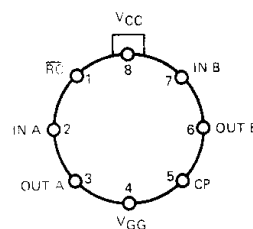
MOS-404

### ORDERING INFORMATION

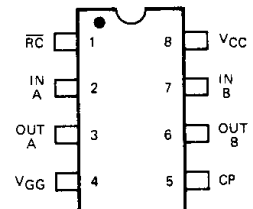
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2809PC
TO-5	0°C to +70°C	AM2809HC
TO-5	-55°C to +125°C	AM2809HM

### CONNECTION DIAGRAMS Top Views

Am2809HC  
Am2809HM



Am2809PC



MOS-405

**MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
DC Input Voltage with Respect to $V_{CC}$	-20V to +0.3V

**OPERATING RANGE**

Part Number	Ambient Temperature	$V_{CC}$	$V_{GG}$
Am2809PC Am2809HC	0°C to +70°C	5.0V ±5%	-12V ±5%
Am2809HM	-55°C to +125°C	5.0V ±5%	-12V ±5%

**ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE** (Unless Otherwise Noted)

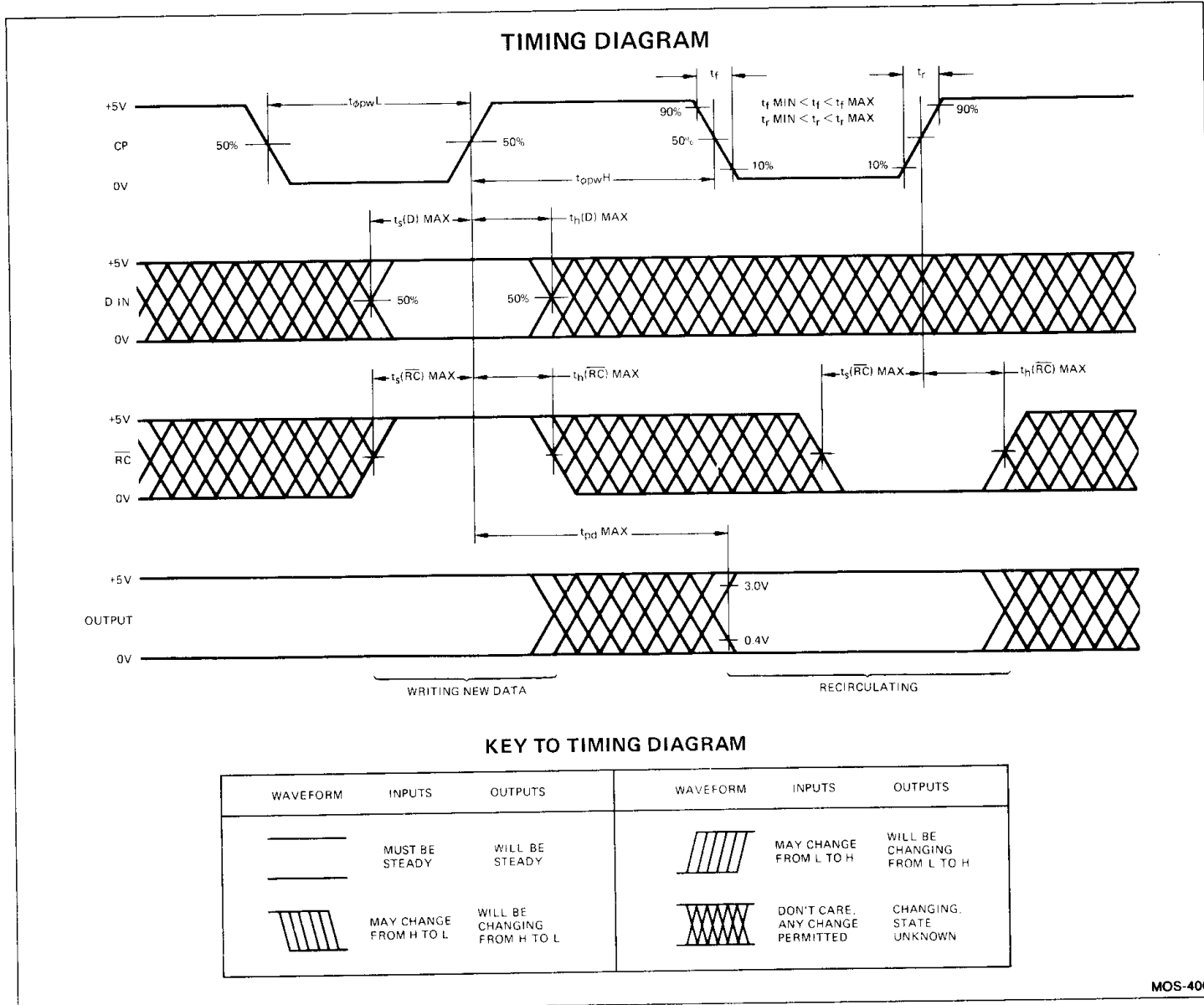
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -0.1\text{mA}$	$V_{CC} - 1.5$			Volts
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.}, I_{OL} = 1.6\text{mA}$		-4	0.4	Volts
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	$V_{CC} - 1$		$V_{CC} + 0.3$	Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			$V_{CC} - 3.95$	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0, T_A = 25^\circ\text{C}$		10	500	nA
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.4\text{V}, T_A = 25^\circ\text{C}$		10	500	nA
$I_{GG}$	Power Supply Current	$f = 2.5\text{MHz}, T_A = 25^\circ\text{C}$		24	32	mA
		$V_{CC} = \text{MAX.}, T_A = 0^\circ\text{C to } +70^\circ\text{C}$			38	
		$f = 2.0\text{MHz}, T_A = -55^\circ\text{C to } +125^\circ\text{C}$			44	

Note: 1. Typical Limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

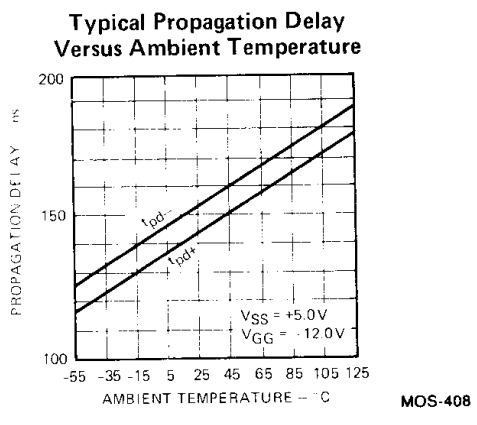
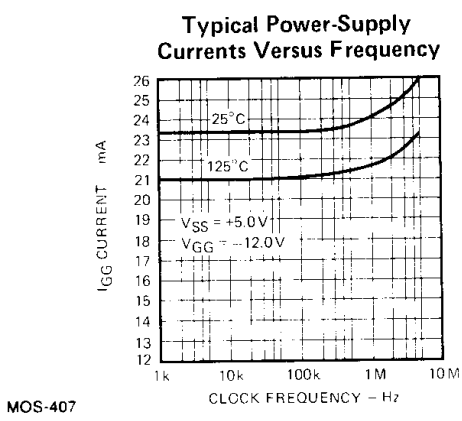
Parameters	Description	Test Conditions	Am2809PC Am2809HC			Am2809HM			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$f_c$	Clock Frequency Range		0		2.5	0		2.0	MHz
$t_{\phi\text{pw}H}$	Clock HIGH Time		0.2		$\infty$	0.25		$\infty$	$\mu\text{s}$
$t_{\phi\text{pw}L}$	Clock LOW Time		0.2		100	0.25		100	$\mu\text{s}$
$t_r, t_f$	Clock Rise and Fall Times	10% to 90%			1.0			1.0	$\mu\text{s}$
$t_s(D)$	Set-up Time, Data Input (see definitions)	$t_r = t_f = 50\text{ns}$	75			100			ns
$t_h(D)$	Hold Time, Data Input (see definitions)	$t_r = t_f = 50\text{ns}$	50			65			ns
$t_s(\overline{RC})$	Set-up Time, Recirculate Control (see definitions)	$t_r = t_f = 50\text{ns}$	50			100			ns
$t_h(\overline{RC})$	Hold Time, Recirculate Control (see definitions)	$t_r = t_f = 50\text{ns}$	50			65			ns
$t_{pd}$	Delay, Clock to Data Out			170	300		170	350	ns
$C_{in}$	Capacitance, Any Input (Note 2)	$f = 1\text{MHz}, V_{IN} = V_{CC}$		3	7		3	7	pF

Note: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.



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### CHARACTERISTIC CURVES

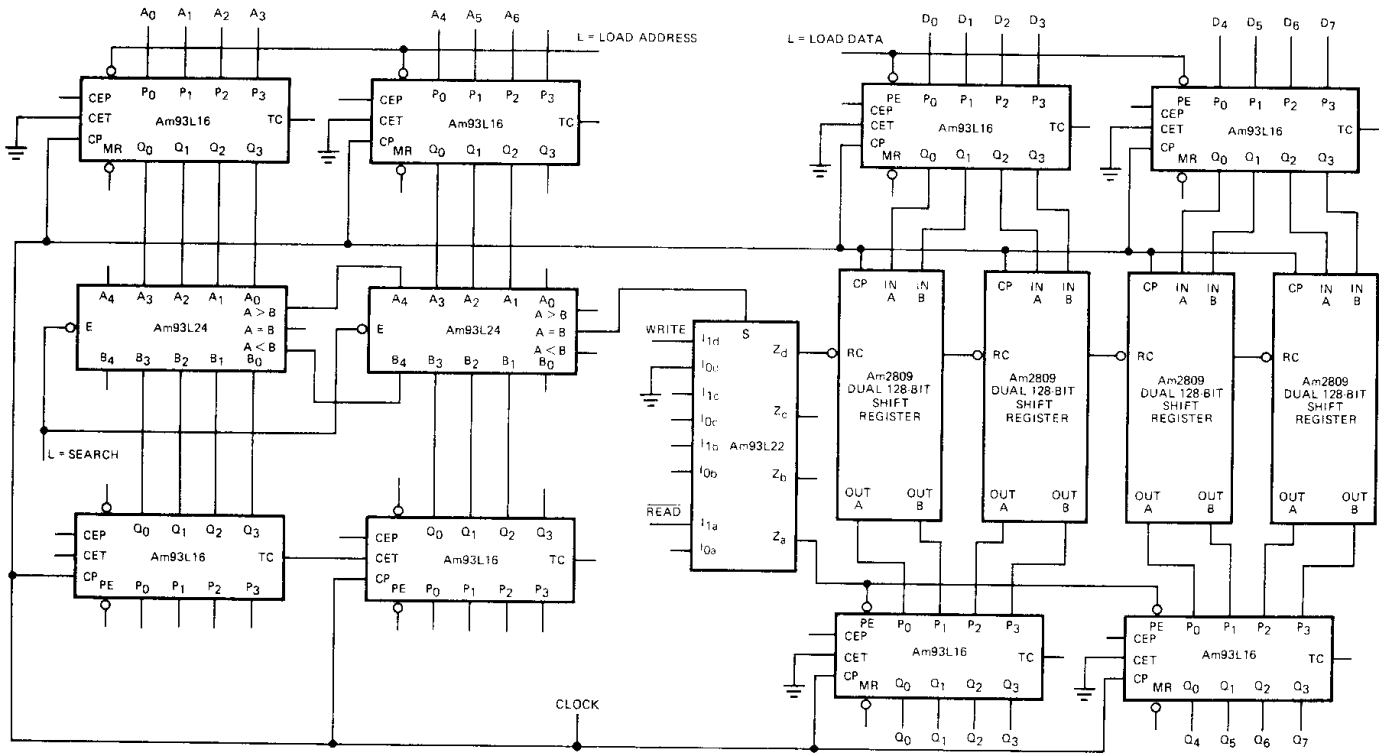


### DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS

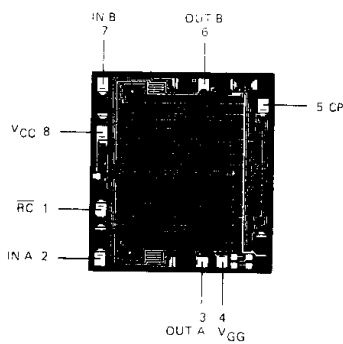


128-Word x 8-Bit Pseudo-Random Access Memory

Data stored in the four dual 128-bit shift registers can be accessed randomly by comparing the desired address with the address currently available at the shift register I/O. A pair of Am93L16 low-power counters keeps track of data addresses as the data circulates around the memory. Other Am93L16 counters are used as 4-bit registers with enables by grounding the count enables. They are used to store the requested address, the new data to be written into the memory, and the data read from the memory. The Am93L24 comparators switch the memories from the recirculate mode to the write mode to enter new data in a write operation. Similarly, the output storage registers are enabled when the Am93L24s indicate comparison in a read operation.

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Metalization and Pad Layout



86 X 95 Mils